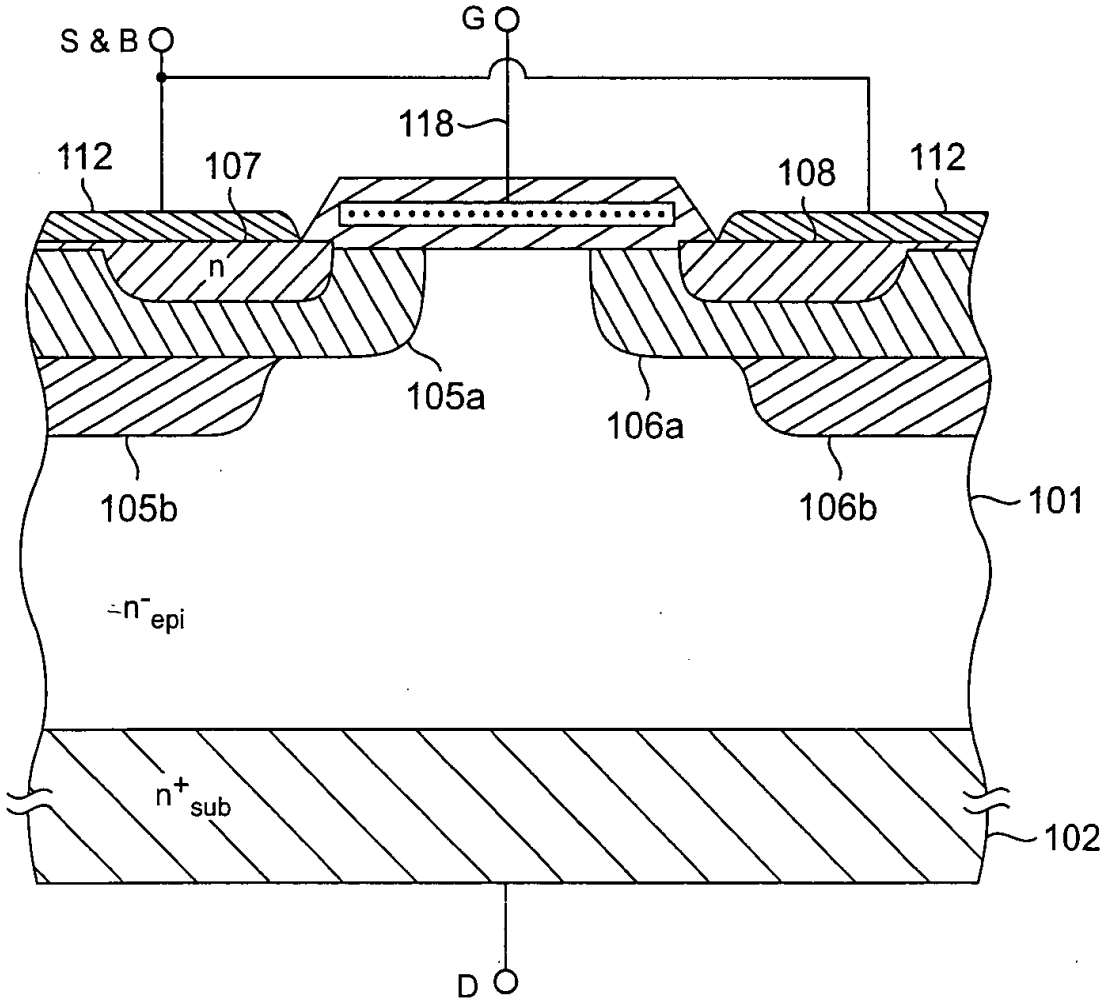
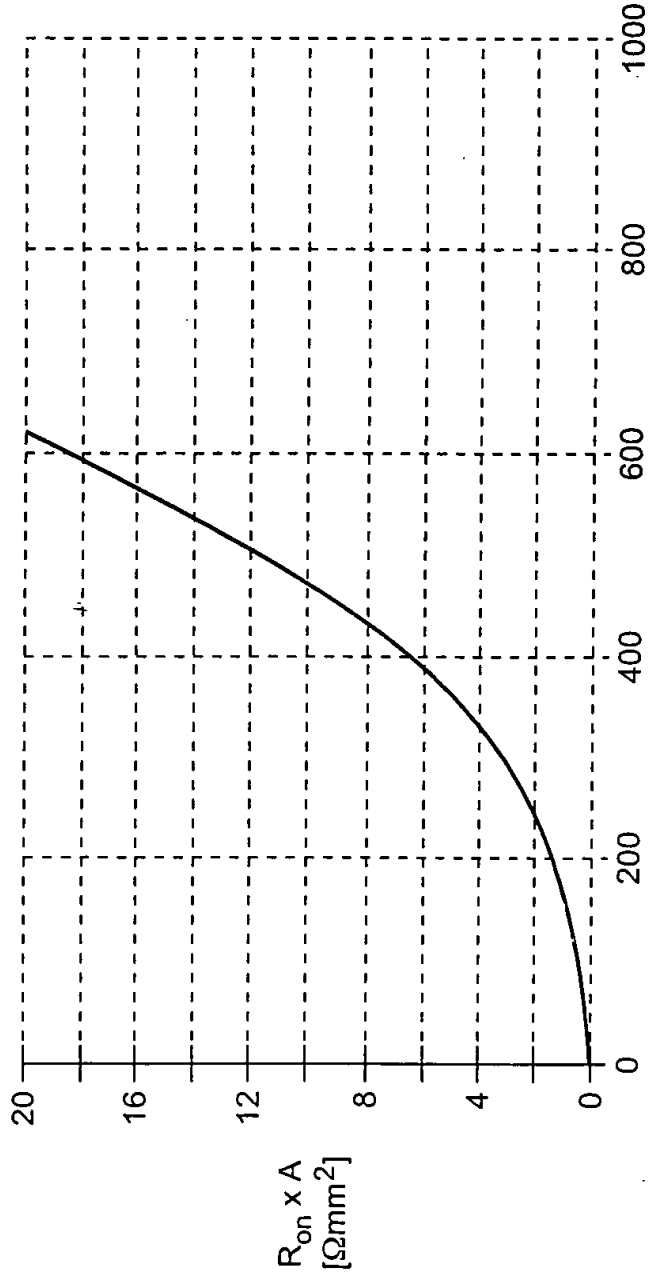



CONVENTIONAL MOSFET

FIG. 1




THE SPECIFIC ON-RESISTANCE OF A VERTICAL DMOS TRANSISTOR WITH THE DOPANT DISTRIBUTION OF FIG. 1

**FIG. 2**

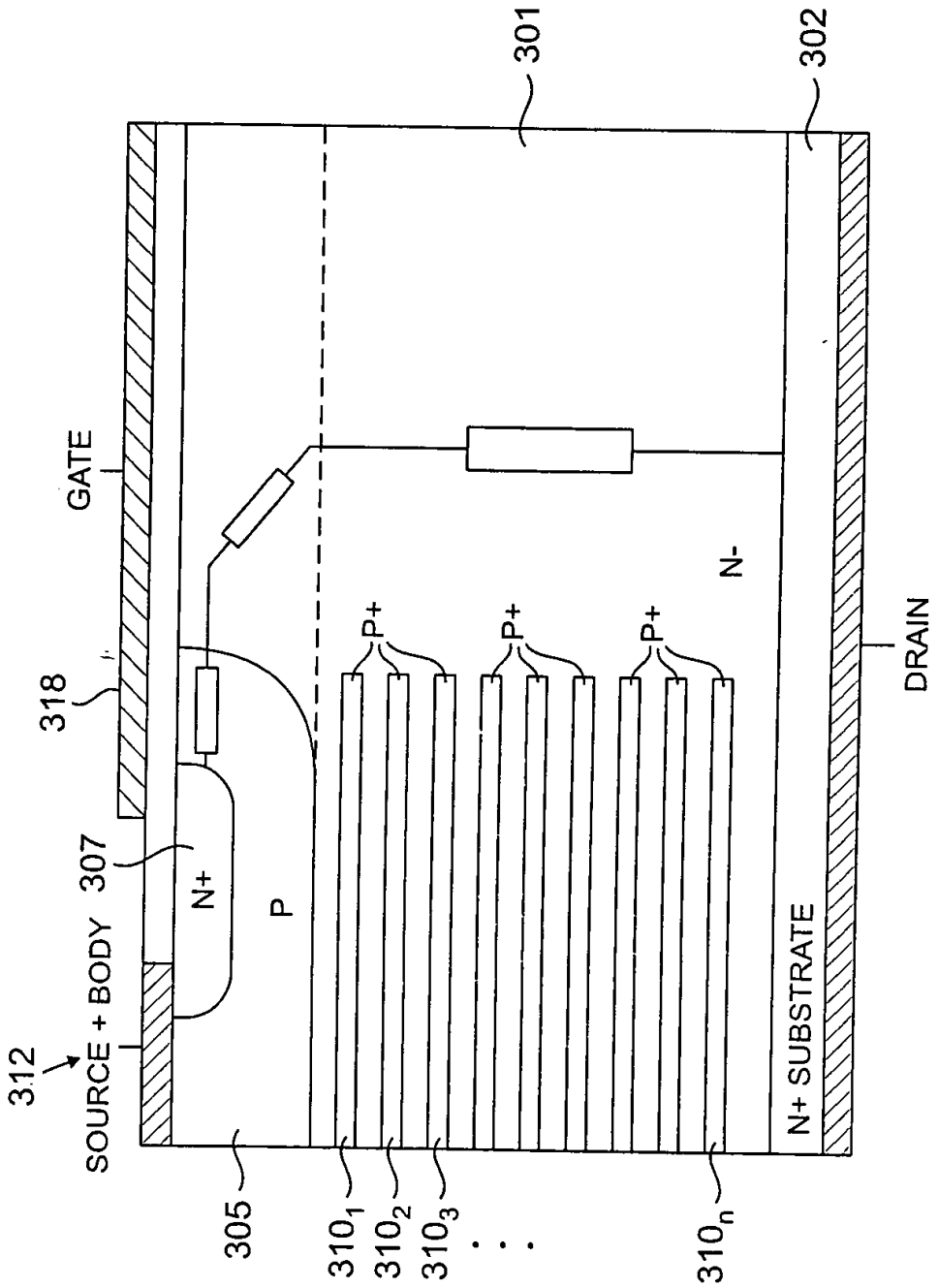

301
302
GATE
318
307
N+
P
P+
P+
P+
N-
DRAIN
312
SOURCE + BODY
N+ SUBSTRATE
305
$310_1$
$310_2$
$310_3$
$310_n$

FIG. 3

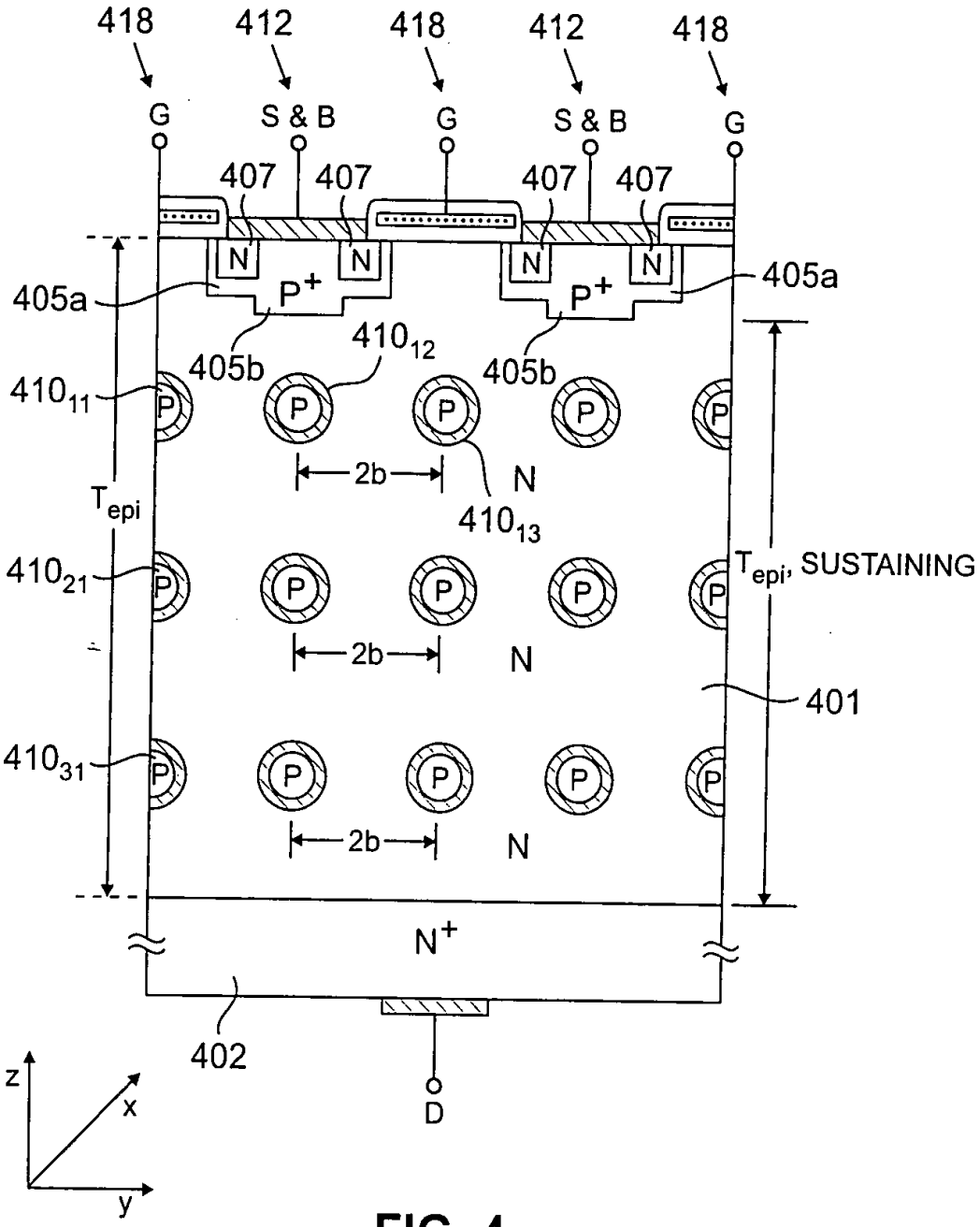

418
412
418
412
418
G
S & B
G
S & B
G
407
407
407
407
N
N
N
N
P+
P+
405a
405a
405b
405b
410$_{12}$
410$_{11}$
P
2b
N
410$_{13}$
T$_{epi}$
410$_{21}$
T$_{epi}$, SUSTAINING
401
410$_{31}$
N+
402
D
z
x
y

FIG. 4

STEP

1. EPITAXIAL DEPOSITION
2. FORM BARRIER LAYER
3. MASK AND ETCH BARRIER LAYER
4. ETCH THE TRENCH

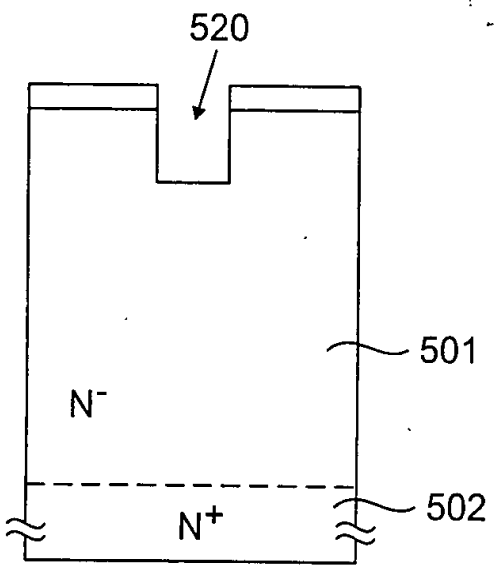



FIG. 5(a)

STEP

5. GROW AN OXIDE LAYER
6. IMPLANT DOPANT

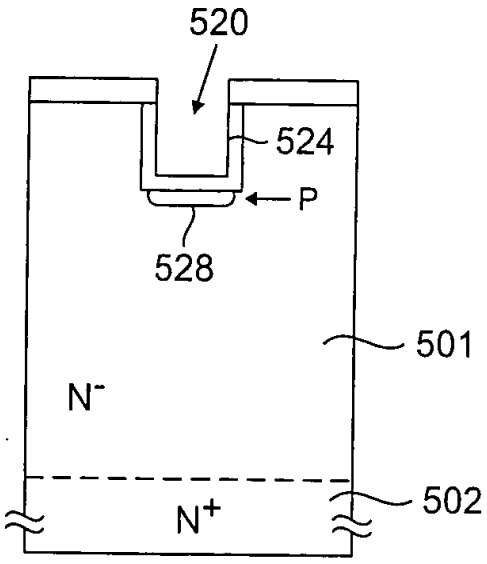



FIG. 5(b)

STEP

7. HIGH TEMPERATURE DIFFUSION
8. ETCH OXIDE AT TRENCH BOTTOM

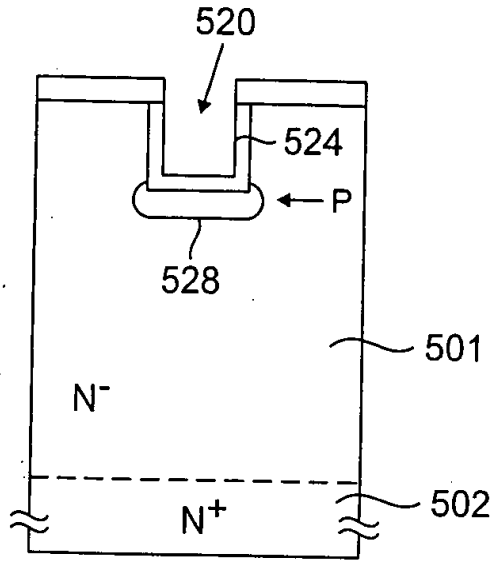



FIG. 5(c)

STEP

9. REPEAT THE TRENCH ETCH STEP, THE OXIDE GROWTH STEP, THE DOPANT INTRODUCTION STEP, THE DRIVE-IN STEP, AND THE OXIDE ETCH STEP AS MANY TIMES AS REQUIRED

10. PERFORM THE OXIDE GROWTH STEP, THE DOPANT INTRODUCTION STEP, THE DRIVE-IN STEP, AND THE OXIDE ETCH STEP FOR THE LAST FLOATING ISLAND LAYER

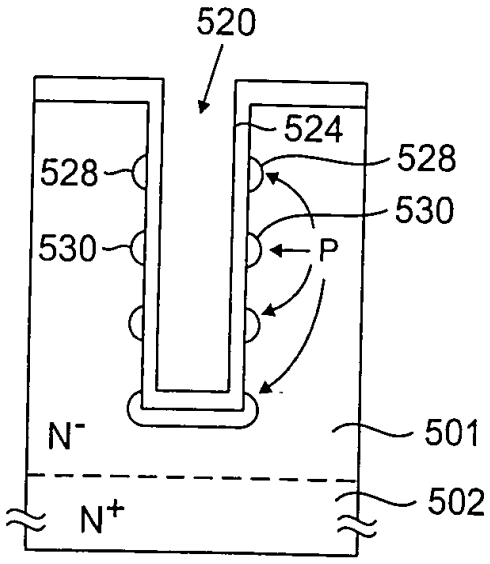



FIG. 5(d)

STEP

11. REMOVE THE OXIDE FROM THE TRENCH BOTTOM TRENCH ETCH (THROUGH THE DIFFUSED P-TYPE LAYER)

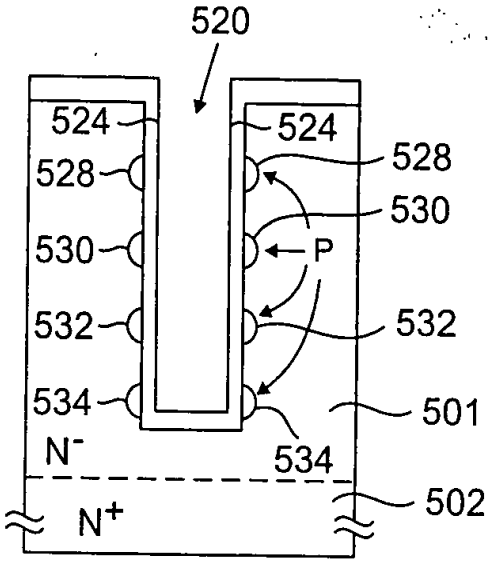



FIG. 5(e)

STEP

12. FILL THE TRENCH

13. PLANARIZE THE WAFER

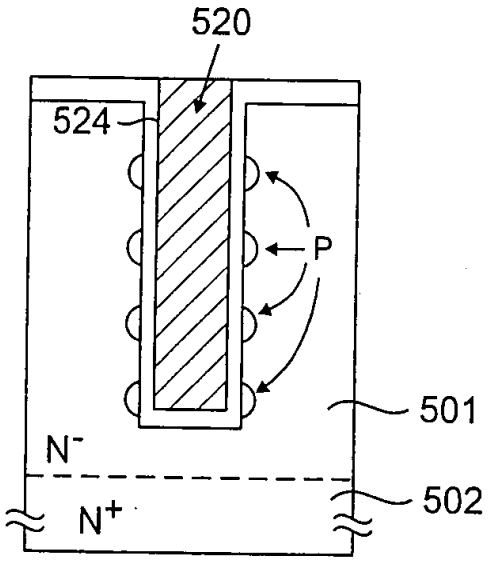



FIG. 5(f)